AMENDMENTS TO THE CLAIMS

Please amend the claims as indicated hereafter. It is believed that the following amendments and additions add no new matter to the present application.

In the Claims: [Use ~~strikethrough~~ for deleted matter (or double square brackets "[[]]" if the strikethrough is not easily perceivable, *i.e.*, "4" or a punctuation mark) and <u>underlined</u> for added matter.]

1. (Currently amended) A signal processing system configured to produce a divider output signal, the system comprising:

a plurality of storage elements;

where each of the plurality of storage elements is configured to receive a first input, a second input, and a reference input signal, and is configured to provide a storage element output;

where <u>the</u> ~~a~~ divider output signal is obtained from at least one storage element output;

where a storage element output from each of the plurality of storage elements is used to provide at least one input to another one of the plurality of storage elements; and

where the storage element output from each of the plurality of storage elements is responsive to the storage element output from at least another one of the plurality of storage elements,

where the divider output signal has a period substantially equal to a period of the reference input signal multiplied by a frequency division ratio, where the frequency division ratio is equal to a total number of the plurality of storage elements,

where a phase difference between a first storage element output and a second

storage element output is equal to 360° divided by twice the ~~a~~ total number of ~~storage elements included in~~ the plurality of storage elements, and

where the signal processing system is implemented in a mobile communications device.

2. (Canceled)

3. (Previously presented) The signal processing system of claim 1, where with respect to each of the plurality of storage elements, a state of the first input is stored in the storage element at a first point in time.

4. (Original) The signal processing system of claim 3, where a state of the storage element output at a second point in time subsequent to the first point in time is equal to the state of the first input stored in the storage element at the first point in time.

5. (Canceled)

6. (Original) The signal processing system of claim 1, where the divider output signal is obtained by combining two storage element outputs.

7. (Original) The signal processing system of claim 6, where a phase difference between a third harmonic component contained in a first storage element and a third harmonic contained in a second storage element is substantially 180°.

8. (Currently amended) The signal processing system of claim 7, where ~~a~~ the third harmonic component contained in ~~a~~ the first storage element output cancels out ~~a~~ the third harmonic component contained in ~~a~~ the second storage element output after the first storage element output and the second storage element output are combined.

9. (Original) The signal processing system of claim 8, where the divider output signal has a duty cycle substantially equal to 50%.

10. (Original) The signal processing system of claim 1, where the reference input signal is a local oscillator signal.

11. (Previously presented) The signal processing system of claim 1, where the signal processing system is a frequency divider.

12. (Canceled)

13. (Currently amended) A method for producing a frequency divider output signal, comprising:

configuring each of a plurality of storage elements to receive a first input, a second input, and a reference input signal, and to provide a storage element output;

obtaining a divider output signal from at least one of the storage element outputs, the divider output signal having a period substantially equal to a period of the reference input signal multiplied by a frequency division ratio, the frequency division ratio being equal to a total number of the plurality of storage elements; and

using the storage element output from each of the plurality of storage elements as

an input to another one of the plurality of storage elements,

where a phase difference between a first storage element output and a second storage element output is equal to 360° divided by twice the total number of ~~storage elements included in~~ the plurality of storage elements, and

where the method is implemented in a mobile communications device.

14. (Canceled)

15. (Previously presented) The method of claim 13, where with respect to each of the plurality of storage elements, a state of the first input is stored in the storage element at a first point in time.

16. (Original) The method of claim 15, where a state of the storage element output at a second point in time subsequent to the first point in time is equal to the state of the first input stored in the storage element at the first point in time.

17. (Canceled)

18. (Original) The method of claim 13, where the divider output signal is obtained by combining two storage element outputs.

19. (Original) The method of claim 18, where a phase difference between a third harmonic component contained in a first storage element and a third harmonic contained in a second storage element is substantially 180°.

20. (Currently amended) The method of claim 19, where ~~a~~ the third harmonic component contained in ~~a~~ the first storage element output cancels out ~~a~~ the third harmonic component contained in ~~a~~ the second storage element output.

21. (Original) The method of claim 13, where the divider output signal has a duty cycle substantially equal to 50%.

22. (Previously presented) The method of claim 13, where the reference input signal is a local oscillator signal.

23. (Previously presented) The method of claim 13, where the method is implemented by a frequency divider.

24. (Canceled)

25. (Currently amended) A signal processing system configured to produce a divider output signal having a period substantially equal to three times a period of a reference input signal, the signal processing system comprising:

a first storage element;

a second storage element; and

a third storage element;

where each of the three storage elements is configured to receive a first input, a second input, and a reference input signal, and is configured to provide a storage element output;

where the divider output signal is obtained from at least one storage element output, where the divider output signal is obtained by combining two of the three storage element outputs; and

where ~~a~~ the storage element output from each of the three storage elements is used to provide at least one input to another one of the three storage elements, where a phase difference between the output of the first storage element and the output of the second storage element is substantially equal to 60° , where a phase difference between a third harmonic component contained in the first storage element output and a third harmonic contained in the second storage element output is substantially 180°, where the third harmonic component contained in the first storage element output cancels out the third harmonic component contained in the second storage element output, and where the signal processing system is implemented in a mobile communications device.

26. (Original) The signal processing system of claim 25, where each of the three storage elements comprises a plurality of transistors.

27. (Original) The signal processing system of claim 26, where with respect to each of the three storage elements, a state of the first input is stored in the storage element at a first point in time.

28. (Original) The signal processing system of claim 27, where a state of the storage element output at a second point in time subsequent to the first point in time is equal to the state of the first input stored in the storage element at the first point in time.

29-32. (Canceled)

33. (Previously presented) The signal processing system of claim 25, where the divider output signal has a duty cycle substantially equal to 50%.

34. (Previously presented) The signal processing system of claim 25, where the reference input signal is a local oscillator signal.

35. (Previously presented) The signal processing system of claim 25, where the signal processing system is a frequency divider.

36. (Canceled)

37. (Currently amended) A method for producing a frequency divider output signal having a period substantially equal to three times a period of a reference input signal, comprising:

configuring each of three storage elements to receive a first input, a second input, and a reference input signal, and to provide a storage element output;

obtaining ~~the~~ a frequency divider output signal from at least one storage element output, where the frequency divider output signal is obtained by combining two of the three storage element outputs; and

using ~~a~~ the storage element output from each of the three storage elements as an input to another one of the three storage elements, where a phase difference between the output of the first storage element and the output of the second storage element is substantially equal to 60°, where a phase difference between a third harmonic component contained in the first storage element output and a third harmonic component contained in the second storage element output is substantially 180°, where ~~a~~ the third harmonic component contained in the first storage element output cancels out ~~a~~ the third harmonic component contained in the second storage element output, and where the method is implemented in a mobile communications device.

38. (Original) The method of claim 37, where each of the three storage elements comprises a plurality of transistors.

39. (Original) The method of claim 38, where with respect to each of the three storage elements, a state of the first input is stored in the storage element at a first point in time.

40. (Original) The method of claim 39, where a state of the storage element output at a second point in time subsequent to the first point in time is equal to the state of the first input stored in the storage element at the first point in time.

41-44. (Canceled)

45. (Currently amended) The method of claim 37, where the <u>frequency</u> divider output signal has a duty cycle substantially equal to 50%.

46. (Previously presented) The method of claim 37, where the reference input signal is a local oscillator signal.

47. (Canceled)